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Search History

DATE: Thursday, July 22, 2004 Printable Copy Create Case

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L7	L3 same l1	8	L7
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L5	L2 and l3	2	L5
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L2	L1 near4 interface	225	L2
L1	self-test$ or bist	7000	L1

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L5: Entry 2 of 2 File: USPT Dec 17, 2002

DOCUMENT-IDENTIFIER: US 6496429 B2
TITLE: Semiconductor memory device

Detailed Description Text (88):
In the above description, both the built-in self-test circuit and the test interface circuit are used. In the system LSI, however, only one of the test interface circuit and the built-in self-test circuit may be disposed.

Detailed Description Text (89):
When built-in self-test (BIST) circuit or test interface circuit (TIC) is alternatively used, the voltage level of repair analyzer enable signal RAen may be set fixedly by mask interconnection or the like in accordance with the use. When both the BIST circuit and test interface circuit (TIC) are used, it is sufficient to set repair analyzer enable signal RAen to the L level as a default and to set repair analyzer enable signal RAen to the H level when BIST circuit performs a test.

Detailed Description Text (93):
The present invention can be also applied to a DDR (Double Data Rate) DRAM in which data is input/output synchronously with both the rising and falling edges of a clock signal. The present invention can be also readily applied to a DDR DRAM, with the configuration in which, as data an input/output latch circuit, a latch circuit for transferring data at the rising edge of a clock signal and a latch circuit for transferring data at the falling edge of the dock signal are provided in parallel with each other and are alternately made activate.